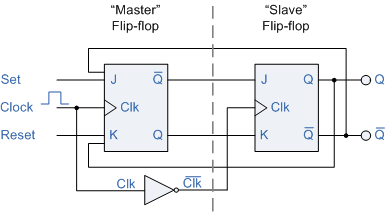
There are two general methodologies for making flip-flops

1. **Edge-triggered**
2. **Master-Slave**

**Master Slave SR flip-flop**

Master-slave flip flop is designed using two separate flip flops. Out of these, one acts as the master and the other as a slave. The overall circuit is known as master- slave flip-flop. The figure of a master-slave J-K flip flop is shown below.



The outputs from Q and Q’ from the “Slave” flip-flop are fed back to the inputs of the “Master” with the outputs of the “Master” flip flop being connected to the two inputs of the “Slave” flip flop. This feedback configuration from the slave’s output to the master’s input gives the characteristic toggle of the JK flip flop as shown below.

The input signals J and K are connected to the gated “master” SR flip flop which “locks” the input condition while the clock (Clk) input is “HIGH” at logic level “1”. As the clock input of the “slave” flip flop is the inverse (complement) of the “master” clock input, the “slave” SR flip flop does not toggle. The outputs from the “master” flip flop are only “seen” by the gated “slave” flip flop when the clock input goes “LOW” to logic level “0”.

When the clock is “LOW”, the outputs from the “master” flip flop are latched and any additional changes to its inputs are ignored. The gated “slave” flip flop now responds to the state of its inputs passed over by the “master” section.

Let’s consider the following figure as well.

